Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (cancelled).

2. [[The]] A phase interpolator ~~as claimed in claim 1,~~ for adjusting a phase of differential clock signals of a receiver to a phase of a data from a transmitter, the phase interpolator comprising:

an integrator configured to slew output signals of a mixer connectable to the interpolator, the mixer outputting said differential clock signals and configured to change swings of the differential clock signals to change capacitance in the integrator upon receiving a signal from a controller ~~edges of differential clock signals adjusted to the phase of the data from the transmitter~~;

[[a]] an output buffer configured to amplify ~~an~~ output signals of the integrator,

a duty cycle correction circuit configured to receive the amplified signals from the output buffer and adjust duty ratios of the output signals of the output buffer to output ~~feed duty correction signals back to the~~ adjusted differential clock signals; and

the controller configured to receive the adjusted differential clock signals and determine whether or not voltages of the adjusted differential signals are amplifiable by the output buffer, the controller configured to output the signal to the integrator to change capacitance of the integrator ~~ensure operations of an amplitude of the output buffer and a data read circuit in adjusting swings and duties of the adjusted differential clock signals~~,

wherein the controller comprises: a first comparison unit configured to determine whether or not the adjusted differential clock signals and the swings of the differential clock signals satisfy a standard voltage that the output buffer is able to amplify,

wherein an output of the first comparison unit is coupled to a capacitor and an inverter to switch the inverter when a voltage of the output of the first comparison unit reaches a predetermined voltage, wherein an output of the inverter is coupled to a gate of an NMOS transistor, wherein the NMOS transistor is coupled to the capacitor in the integrator and the adjusted differential clock signal, wherein the integrator is configured to change a capacitance of [[the]] a capacitor in the integrator in accordance with switching the gate of the NMOS transistor.

3. (currently amended) The phase interpolator as claimed in claim [[1]] 2, wherein the controller comprises:

a second comparison unit configured to determine whether or not the adjusted differential clock signals and the swings of the differential clock signals satisfy a predetermined voltage that the output buffer is able to amplify;

a third comparison unit configured to generate a clock using the adjusted differential clock signals;

wherein an output of the second comparison unit is coupled to a data input of a first flip-flop,

wherein an output of the third comparison unit is coupled to a delay circuit configured to generate a delayed clock signal from the output of the third comparison unit,

wherein the first flip-flop receives the delayed clock signal to [[hit]] process the output of the second comparison unit to output an output signal,

wherein a data input of a second flip-flop and a NAND gate receives the output signal,

wherein a clock input of the second flip-flop receives delayed clock signal and [[hits]] processes the output of the first flip-flop to output [[it]] a second output signal to the NAND gate,

wherein an output of the NAND gate is coupled to a gate of an NMOS transistor,

wherein the NMOS transistor is coupled to [[a]] the capacitor in the integrator and the adjusted differential clock signal,

wherein the integrator is configured to change a capacitance in the integrator to switch the gate of the NMOS transistor off when a differential voltage of the adjusted differential clock signal is smaller than a predetermined voltage.

4. (original) The phase interpolator as claimed in claim 2, wherein the first comparison unit comprises:

a fourth comparison unit including:

a positive input port configured to receive a first signal;

a negative input port configured to receive a second signal; and

a reference input port configured to receive a third signal;

a fifth comparison unit including:

a positive input port configured to receive the second signal;

a negative input port configured to receive the first signal; and

a reference input port configured to receive the third signal; and

an EXOR gate configured to receive an output of the fourth comparison unit and fifth comparison unit to output an exclusive OR operation of the fourth comparison unit and fifth comparison unit.

5. (currently amended) The phase interpolator as claimed in claim 4, wherein the fourth comparison unit and the fifth comparison unit ~~comprises~~ comprise:

a sixth comparison unit including:

a positive input port configured to receive a fourth signal; and

a negative input port configured to receive a fifth signal;

a seventh comparison unit including:

a positive input port configured to receive an output of the sixth comparison unit; and

a negative input port configured to receive a sixth signal; and

an inverter configured to receive an output of the seventh comparison unit to invert the output of the seventh comparison unit.

6. (original) The phase interpolator as claimed in claim 4, wherein the controller includes a circuit configured to control the capacitance in the integrator, so as not to allow the swings to drop lower than a predetermined value.

7. (currently amended) The phase interpolator as claimed in claim [[1]] 2, wherein the controller comprises a first operational amplifier configured to determine whether or not the swings of the adjusted differential clock signals and the differential clock signals are amplifiable by the output buffer,

wherein an output of the first operational amplifier is coupled to [[a]] the capacitor and [[an]] the inverter,

~~wherein the inverter switches at a predetermined voltage, an output of the inverter is coupled to a gate of an NMOS transistor, the NMOS transistor is coupled to the capacitor and the adjusted differential clock signal, wherein the integrator is configured to change the capacitance of the capacitor in the integrator according to switching the gate of the NMOS transistor,~~

wherein the first operational amplifier comprises:

a second operational amplifier including:

a positive input port configured to receive a first differential clock signal;

a negative input port configured to receive a second differential clock signal; and

a reference input port configured to receive a reference signal;

a third operational amplifier including:

a positive input port configured to receive the second differential clock signal;

a negative input port configured to receive the first signal; and

a reference input port configured to receive the reference signal; and

an EXOR gate configured to receive an output of the second operational amplifier and third operational amplifier to output an exclusive OR operation of the second operational amplifier and third operational amplifier,

wherein the second and third operational amplifier comprise:

a fourth operational amplifier configured to output a comparison signal, the fourth operational amplifier including:

a positive input port configured to receive the first differential clock signal; and

a negative input port configured to receive the second differential clock signal;

a fifth operational amplifier including:

a positive input port configured to receive the comparison signal; and

a negative input port configured to receive the reference signal; and

an inverter configured to receive an output of the fifth operational amplifier to invert the output of the fifth operational amplifier.

8. (currently amended) The phase interpolator as claimed in claim [[1]] 2, wherein the controller comprises:

a first ~~sixth~~ operational amplifier configured to determine whether or not adjusted differential clock signals and the swings of the differential clock signals satisfy a predetermined voltage that the output buffer is able to amplify;

a second ~~seventh~~ operational amplifier configured to generate a clock using the adjusted differential clock signals;

wherein an output of the first ~~sixth~~ operational amplifier is coupled to a data input of a ~~third~~ first flip-flop, wherein an output of the second ~~seventh~~ operational amplifier is coupled to a delay circuit configured to generate a delayed clock signal from the output of the second ~~seventh~~

operational amplifier, wherein the first ~~third~~ flip-flop receives the delayed clock signal to hit the output of the first ~~sixth~~ operational amplifier to output an output signal, wherein a data input of a ~~fourth~~ second flip-flop and a NAND gate receives the output signal, wherein a clock input of the second ~~fourth~~ flip-flop receives delayed clock signal and ~~hits~~ processes the output of the first flip-flop to output [[it] a second output signal to the NAND gate, wherein an output of the NAND gate is coupled to a gate of [[an]] the NMOS transistor, ~~wherein the NMOS transistor is coupled to a capacitor in the integrator and the adjusted differential clock signal~~, wherein the integrator is configured to change the capacitance of the capacitor in the integrator to switch the gate of the NMOS transistor off when a differential voltage of the adjusted differential clock signals is smaller than a predetermined voltage,

wherein the first ~~sixth~~ and second ~~seventh~~ operational amplifier comprise:

a third ~~eighth~~ operational amplifier including:

a positive input port configured to receive a first differential clock signal;

a negative input port configured to receive a second differential clock signal; and

a reference input port configured to receive a reference signal,

a fourth ~~ninth~~ operational amplifier including:

a positive input port configured to receive the second differential clock signal;

a negative input port configured to receive the first differential clock signal; and

a reference input port configured to receive the reference signal; and

an EXOR gate configured to receive an output of the third ~~eighth~~ operational amplifier and the fourth ~~ninth~~ operational amplifier to output an exclusive OR operation of the third ~~eighth~~ operational amplifier and the fourth ~~ninth~~ operational amplifier,

wherein the third ~~eighth~~ and fourth ~~ninth~~ operational amplifier comprise:

a fifth ~~tenth~~ operational amplifier including:

a positive input port configured to receive the first differential clock; and

a negative input port configured to receive the second differential clock;

a sixth ~~eleventh~~ operational amplifier including:

a positive input port configured to receive an output of the fifth ~~tenth~~ operational amplifier; and

a negative input port configured to receive the reference signal; and

an inverter configured to receive an output of the sixth ~~eleventh~~ operational amplifier to invert the output of the sixth ~~eleventh~~ operational amplifier.

9. (currently amended) A phase interpolator comprising:

an integrator configured to receive output signals of a mixer connectable to the interpolator ~~adjusted differential clock signals, the integrator~~ and configured to slew [[the]] differential clock signals outputting from the mixer;

[[a]] an output buffer configured to amplify an output of the integrator;

a duty cycle correction circuit configured to receive amplified signals from the output buffer to adjust a duty ratio ~~phases~~ of the amplified signals, the duty cycle correction circuit configured to output ~~feed~~ the adjusted signals ~~back~~ to the output buffer, and

a controller configured to control a rate of slewing the differential clock signals carried out by the integrator, when swings of the differential clock signals are below a predetermined value.

10. (currently amended) The phase interpolator as claimed in claim 9, wherein the controller comprises:

a first comparison unit configured to receive the adjusted differential clock signals and a first reference signal to compare a difference between the adjusted differential clock signals with the first reference signal, the first comparison unit configured to output a first detection signal when the difference is smaller than the first reference signal; and

a first inverter configured to receive the first detection signal in order to invert the first detection signal.

11. (original) The phase interpolator as claimed in claim 10, wherein the controller comprises a

first capacitor configured to store electrical charges of the first detection signal, wherein the first inverter switches the output signal when an output node coupled to the first capacitor reaches a predetermined voltage.

12. (currently amended) The phase interpolator as claimed in claim 11, wherein the integrator comprises:

a second capacitor; and

a switching circuit coupled to the second capacitor, the switching circuit configured to control the second capacitor according to an output of the first inverter.

13. (original) The phase interpolator as claimed in claim 12, wherein the switching circuit is a transistor, wherein the integrator further comprises a third capacitor coupled to a drain of the transistor.

14. (currently amended) The phase interpolator as claimed in claim 10, wherein ~~at least one of~~ the first~~, second, and third~~ comparison unit, ~~comprise~~ comprises:

a second ~~fourth~~ comparison unit configured to receive a first voltage according to a first signal of the differential clock signals ~~signal~~, a second voltage according to a second signal of the differential clock signals ~~signal,~~ and a reference voltage ~~according to a reference signal~~ according to a reference signal to compare a voltage ~~that is that is subtracted~~ subtracts the second voltage from the first voltage with the reference voltage;

a third ~~fifth~~ comparison unit configured to receive the first voltage, the second voltage, and the reference voltage in order to compare a voltage that is the first voltage subtracted from the second voltage with the reference voltage; and

an EXOR gate configured to receive the ~~output~~ outputs of the ~~fourth~~ second and ~~fifth~~ third comparison ~~unit~~ units to output an exclusive OR operation of the ~~output~~ outputs of the ~~fourth~~ second and ~~fifth~~ third comparison ~~unit~~ units.

15. (currently amended) The phase interpolator as claimed in claim 14, wherein at least one of the fourth and fifth comparison unit comprise:

a fourth ~~sixth~~ comparison unit configured to receive the first and second ~~voltage~~ voltages to output a voltage that is ~~subtracted~~ a subtraction of the second voltage from the first voltage;

a fifth ~~seventh~~ comparison unit configured to receive an output voltage of the fourth ~~sixth~~ comparison unit and the reference voltage to output a voltage that is ~~subtracted~~ a subtraction of the reference voltage from the output voltage of the fourth ~~sixth~~ comparison unit; and;

a second inverter configured to receive an output of the fifth ~~seventh~~ comparison unit to invert the output of the fifth ~~seventh~~ comparison unit.

16. (currently amended) The phase interpolator as claimed in claim 9, wherein the controller comprises:

a first ~~second~~ comparison unit configured to receive the differential clock signals and a second reference signal to compare a difference between the differential clock signals with the second reference signal, the first ~~second~~ comparison unit configured to output a second detection signal when the difference is smaller than the second reference signal;

a second ~~third~~ comparison unit configured to generate a clock signal using the differential clock signals;

a delay circuit configured to delay an output of the second ~~third~~ comparison unit;

a first flip-flop configured to receive an output of the first ~~second~~ comparison unit as a first data signal and an output of the delay circuit as a first clock signal to output the first data signal at a predetermined timing;

a first ~~second~~ inverter configured to receive the output signal of the delay circuit and to invert the output signal of the delay circuit;

a second flip-flop configured to receive an output of the first flip-flop as a second data signal and an output of the first ~~second~~ inverter as a second clock signal to output the second data signal at a predetermined timing; and

a NAND gate configured to receive the outputs of the first and second flip-flops to output negative AND operation of the outputs of the first and second flip-flops.

17. (currently amended) The phase interpolator as claimed in claim 16, wherein at least one of the first, second, and third comparison ~~unit,~~ units comprise:

a third ~~fourth~~ comparison unit configured to receive a first voltage according to a first signal of the differential clock signals ~~signal~~, a second voltage according to a second signal of the differential clock signals ~~signal~~, and a reference voltage ~~according to a reference signal~~ according to a reference signal to compare a voltage that ~~is subtracted~~ subtracts the second voltage from the first voltage with the reference voltage;

a fourth ~~fifth~~ comparison unit configured to receive the first voltage, the second voltage, and the reference voltage to compare a voltage that ~~is subtracted~~ subtracts the first voltage from the second voltage with the reference voltage; and

an EXOR gate configured to receive the ~~output~~ outputs of the ~~fourth~~ third and ~~fifth~~ fourth comparison ~~unit~~ units to output an exclusive OR operation of the ~~output~~ outputs of the ~~fourth~~ third and ~~fifth~~ fourth comparison ~~unit~~ units.

18. (currently amended) The phase interpolator as claimed in claim 17, wherein at least one of the fourth and fifth comparison ~~unit~~ units comprises:

a fifth ~~sixth~~ comparison unit configured to receive the first and second ~~voltage~~ voltages to output a voltage that ~~is subtracted~~ subtracts the second voltage from the first voltage;

a sixth ~~seventh~~ comparison unit configured to receive an output voltage of the fifth ~~sixth~~ comparison unit and the reference voltage to output a voltage that ~~is subtracted~~ subtracts the reference voltage from the output voltage of the fifth ~~sixth~~ comparison unit; and

a second inverter configured to receive an output of the sixth ~~seventh~~ comparison unit and to invert the output of the sixth ~~seventh~~ comparison unit.

19. (currently amended) A phase interpolator comprising:

a digital-analog converter configured to convert an inputted signal into a current;

a mixer configured to receive an output of the digital-analog converter and a clock, the mixer configured to shift a phase of the clock according to the output of the digital-analog converter to output [[a]] adjusted differential clock signals;

an integrator configured to receive the adjusted differential clock signals~~, the integrator~~ and configured to slew the differential clock signals outputted from the mixer;

[[a]] an output buffer configured to amplify an output of the integrator;

a duty cycle correction circuit configured to receive amplified signals from the output buffer to adjust duty ratios ~~phase~~ of the amplified signals, the duty cycle correction circuit configured to output ~~feed~~ the adjusted signals ~~back~~ to the output buffer; and

a controller configured to control a rate of the slewing the differential clock signals carried out by the integrator, when swings of the differential clock signals are below a predetermined value.

20. (currently amended) A receiver comprising:

a phase interpolator including:

a digital-analog converter configured to convert an inputted signal into a current;

a mixer configured to receive an output of the digital-analog converter and a clock, the mixer configured to shift a phase of the clock according to the output of the digital-analog converter to output adjusted differential clock signals;

an integrator configured to receive data and said adjusted differential clock signals~~, the integrator configured~~ and to slew the adjusted differential clock signals;

[[a]] an output buffer configured to amplify an output of the integrator;

a duty cycle correction circuit configured to receive amplified signals from the output buffer to adjust duty ratios ~~a phase~~ of the amplified ~~signal~~ signals, the duty cycle correction circuit configured to output ~~feed~~ the adjusted signals ~~back~~ to the output buffer; and

a controller configured to control a rate of the slewing of the differential clock signals carried out by the integrator, when swings of the differential clock signals are below a predetermined value; and

a data read unit configured to read [[a]] data using the output of the output buffer.